What is claimed :

1. A flash memory system comprising:
an array of flash memory cells;
four local bit lines positioned generally parallel with each other;
a pair of global bit lines, each global bit line is selectively coupled to a pair of the four local bit lines, wherein the pair of local bit lines are alternately positioned with respect to each other; and
a multiplex circuit to selectively couple the associated local bit lines to the associated global bit lines.

2. The flash memory system of claim 1 wherein the multiplex circuit comprises:
four select transistors coupled between an associated local bit line and an associated global bit line, each select transistor having a control gate.

3. The flash memory system of claim 2 further comprising:
a first select line coupled to control gates of the select transistors that are coupled to a first and a second local bit line of the four local bit lines; and
a second select line coupled to control gates of the select transistors that are coupled to a third and a fourth local bit line of the four local bit lines.

4. The flash memory system of claim 1 wherein the array of flash memory cells is positioned adjacent the multiplex circuit.

5. The flash memory system of claim 1 wherein each of the flash memory cells is comprised of a floating gate capable of holding a charge.

6. The flash memory system of claim 5 wherein a presence or absence of the charge determines a state of the flash memory cell.

7. A flash memory system comprising:

an array of flash memory cells;

a plurality of local bit lines positioned substantially parallel to each other;

a plurality of global bit lines, each global bit line selectively coupled to an even quantity of the plurality of local bit lines, wherein the even quantity of the plurality of local bit lines are not adjacent to each other;

a multiplex circuit comprising four select transistors coupled between an associated local bit line and an associated global bit line, each select transistor having a control gate, the multiplex circuit selectively coupling the associated local bit lines to the associated global bit lines;.

a first select line coupled to control gates of the select transistors that are coupled to a first and a second local bit line of the plurality of local bit lines; and

a second select line coupled to control gates of the select transistors that are coupled to a third and a fourth local bit line of the plurality of local bit lines.

8. The flash memory system of claim 7 wherein there are twice as many of the plurality of local bit lines as global bit lines.

9. The flash memory system of claim 7 wherein each global bit line is selectively coupled to alternating local bit lines.

10. The flash memory system of claim 7 wherein the plurality of local bit lines are formed on a first metal level and the plurality of global bit lines are formed on a second metal level.

11. The flash memory system of claim 7 wherein the system is manufactured such that the plurality of local bit lines are on a different level than the plurality of global bit lines.

12. The flash memory system of claim 7 wherein the array of flash memory cells is floating gate memory cells arranged in rows and columns.

13. A flash memory system comprising:

an array of floating gate memory cells;

a plurality of local bit lines positioned substantially parallel to each other;

a plurality of global bit lines that includes twice as many global bit lines as local bit lines, each global bit line selectively coupled to an even quantity of the plurality of local bit lines such that the plurality of local bit lines coupled to each global bit line are not adjacent to each other; and

a plurality of multiplex circuits, each circuit coupled between an associated local bit line and an associated global bit line.

14. The flash memory system of claim 13 wherein the multiplex circuit comprises:

a plurality of select transistors coupled between an associated local bit line and an associated global bit line, each select transistor having a control gate.

15. The flash memory system of claim 14 and further including a plurality of select lines, each select line coupled to a control gate of a select transistor of the plurality of select transistors.

16. The flash memory system of claim 15 wherein the array of floating gate memory cells is located between a first multiplex circuit and a second multiplex circuit of the plurality of multiplex circuits.

17. The flash memory system of claim 14 wherein the select transistors are located at opposite ends of the array of floating gate memory cells.

18. The flash memory system of claim 14 wherein the plurality of local bit lines is located on a different level than the plurality of global bit lines.

19. The flash memory system of claim 13 wherein at least one local bit line of the plurality of local bit lines is located above a drain diffusion region.

20. The flash memory system of claim 13 wherein the array of floating gate memory cells is arranged in rows and columns.